UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,629	02/13/2004	Todd Brooks	1875.3960001	5354

28393 7590 04/04/2005

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVE., N.W.
WASHINGTON, DC 20005

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,629	BROOKS ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37 and 38* is/are allowed.

6)☒ Claim(s) *1-4,6-19,21,22,24,25,28,29,33-36,39,41-47,49 and 50* is/are rejected.

7)☒ Claim(s) *5,20,23,26,27,30-32,40,48 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 40 is objected because there is no antecedent basis for the limitation "the first, second ...".

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Kim (USP 6744319). Kim discloses in figure 6 an analog circuit comprising: a low noise transconductance cell (712) having a first output node and a second output node; a high swing transconductance cell (714) having a first output node and a second output node; and an output switch (716) having a first input node coupled to the first output node of the low noise transconductance cell, a second input node coupled to the second output node of the low noise transconductance cell, a third input node coupled to the first output node of the high swing transconductance cell, and a fourth input node coupled to the second output node of the high swing transconductance cell, wherein a first and a second output node of the output switch are coupled to the first and second input nodes of the output switch when the low noise transconductance cell is selected and the first and second

output nodes of the output switch are coupled to the third and fourth input nodes of the output switch when the high swing transconductance cell is selected.

3. Claims 33-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto (USP 6552611).

As to claim 33, Yamamoto discloses in figure 9 a circuit comprising: a first half-circuit (17) including a first resistor (Ro1), and a feedback loop having a first input (M41) transistor wherein the feedback loop is configured to keep Vgs of the first input transistor constant (Col. 7, lines 4-12, and Col. 10, lines 43-45); a second half-circuit (18) including a second resistor (Ro2) having a first terminal coupled to a second terminal of the first resistor, and a feedback loop having a second input transistor (M44) coupled to the second resistor wherein the feedback loop is configured to keep Vgs of the second input transistor constant.

As to claim 34, figure 9 shows a first current source (Ib1) coupled to the first input transistor; and a second current source (Ib2) coupled to the second input transistor.

Claims 35-36 recite similar limitations of claims 33 and 34. Therefore, they are rejected for the same reasons.

4. Claims 44-47 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Syrusian et al. (USP 6570447).

As to claim 44, Syrusian et al. discloses in figures 1, 2 and 4 a circuit comprising: a first resistance stage (stage 1 in figure 4), wherein the first resistance stage includes: a first resistor (right R1 in stage 1) having a first and a second terminal, a second resistor (the left R1) having a first and a second terminal, and a first switch (transistor in stage 1) wherein a first terminal of the first switch is coupled to the second terminal of the first resistor and a second terminal of the first

switch is coupled to the second terminal of the second resistor; a second resistance stage (stage 2 in figure 4), wherein the second resistance stage includes: a third resistor (the right R1 in stage 2) having a first and a second terminal, a fourth resistor (the left R1 in stage 2) having a first and a second terminal, and a second switch (the transistor in stage 2) wherein a first terminal of the second switch is coupled to the second terminal of the third resistor and a second terminal of the second switch is coupled to the second terminal of the fourth resistor; and a first feedback loop (38, 22, 24 and 58 in figure 1) coupled to the first terminal of the third resistor and the first terminal of the first resistor; and a second feedback loop (40, 32, 24 and 60 in figure 1) coupled to the first terminal of the fourth resistor and the first terminal of the second resistor.

As to claim 45, figures 1, 2 and 4 shows that the first resistance stage is coupled between the first feedback loop and the second feedback loop when the first switch is closed.

As to claim 46, figure 1, 2 and 4 shows that the second resistance stage is coupled between the first feedback loop and the second feedback loop when the second switch is closed.

As to claim 47, figures 1, 2 and 4 shows a resistor (R0 in figure 2 or figure 4) coupled to the first feedback loop and to the second feedback loop.

Claim 49 recites similar limitations of claims above. Therefore, it is rejected for the same reasons.

5. Claim 50 is rejected under 35 U.S.C. 102(b) as being anticipated by Hirano et al. (USP 5179298).

Hirano et al. discloses in figure 1B a circuit comprising a resistor (R21) having a first and a second terminal; and a feedback loop wherein the feedback loop includes a first input transistor (QP2) receiving an input voltage at its gate and having a source coupled to the first terminal of

the first resistor, a first output transistor (QP4) having a source coupled to the first terminal of the first resistor, and an inverter stage (QP3, QN3) having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides an output current at its drain.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 7-19, 22, 24, 25, 28, 39 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akita et al. (USP 4080828) in view of Wanlass (USP 3356858).

As to claim 1, Akita et al.'s figure 6 shows a circuit comprises first resistor (241); first half circuit (202); and second half circuit (230). Thus, figure 6 shows all limitations of the claim except for the detail of the first and second half circuits. However, Wanlass discloses in figure 5 shows an inverter circuit in which power losses are minimized. Therefore, it would have been obvious to one having ordinary skill in the art to use Wanlass' inverter for each of Akita et al. inverters. Thus, the modified Akita et al.'s figure 6 shows that the first half circuit includes a first input transistor (the PMOS in the modified inverter 221), a first output transistor (the PMOS in the modified 223), and an inverter stage (222); the second half circuit includes a first input transistor (the PMOS in the modified inverter 231), a first output transistor (the PMOS in the modified 233), and an inverter stage (232) (further see the rejection of claim 50).

As to claim 2, the modified Akita et al. shows that the first input voltage is a positive input voltage and the first output current is a negative output current and the second input voltage is a negative input voltage and the second output current is a positive current. (when input of 221 is high, output of 223 is low. Thus, the PMOS transistor in the modified inverter 223 providing negative output current. When input of 231 is low, output of 233 is high. Thus, the PMOS transistor in the modified inverter 233 providing positive output current).

As to claim 3, the modified Akita et al. shows a first current source (the NMOS in the modified 221) coupled to the drain of the first input transistor; and a second current source (the NMOS in modified 223) coupled to the drain of the second input transistor.

As to claim 4, the modified Akita et al. shows a first impedance current source (the NMOS in the modified 221) coupled to the drain of the first input transistor; and a second impedance (the NMOS in modified 223) coupled to the drain of the second input transistor.

As to claim 7, the prior arts show all limitations of the claim except for the wells of the first and second input transistors are respectively connected to the source of each transistor. However, it is notoriously well known that transistor with well connected to it source for reducing leakage current. Therefore, it would have been obvious to one having ordinary skill in the art to connect the wells of the first and second input transistor respectively to the source of each transistor for the purpose of reducing leakage current.

As to claims 8-11, the modified Akita et al.'s figure 6 shows the first and second input transistors, the first and second output transistors are of the same polarity or PMOS.

As to claim 12, the modified Akita et al.'s figure 6 shows that the first half-circuit further comprises a third current source (the NMOS in the modified 223) coupled to the drain of the first

output transistor and the second half-circuit further comprises a fourth current source (the NMOS in the modified 233) coupled to the drain of the second output transistor.

As to claim 13, the modified Akita et al.'s figure 6 shows that the first current source comprises a first current source transistor and the second current source comprises a second current source transistor, and wherein the drain of the first current source transistor is coupled to the drain of the first input transistor and the drain of the second current source transistor is coupled to the drain of the second input transistor.

As to claim 14, the modified Akita et al.'s figure 6 shows that the first and second current source transistors have a common polarity.

As to claim 15, the modified Akita et al.'s figure 6 shows that the first and second current source transistors are NMOS transistors.

Claims 16-19, 22, 24, 25 and 28 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claim 39, the modified Akita et al.'s figure 6 further shows plurality of switchable resistance stages (transistors in the modified 212-213).

As to claim 41, the modified Akita et al.'s figure 6 shows a resistor 241 coupled to the source of the first input transistor and to the source of the second input transistor.

As to claim 42, the modified Akita et al.'s figure 6 shows a current source (the PMOS in the modified 212) coupled to a first terminal of a fifth switch (the NMOS transistor in the modified 212), wherein a second terminal of the fifth switch is coupled to one of the plurality of resistance stages.

As to claim 43, the modified Akita et al.'s figure 6 shows that the current source is coupled to one of the plurality of resistance stages when the fifth switch is closed.

8. Claims 1, 6, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau (USP 5682123) in view of Akita et al. (USP 4080828).

Chau's figure 2A shows a circuit having first half including first resistors (resistor shown in figure 2C); input transistor (the PMOS transistor in the middle inverter 13), first output transistor (the PMOS transistor in the most right inverter 13); an inverter stage (inverter between the middle and the most right inverters); and a first bias current source (transistor 19 in figure 2C) coupled to the first terminal of the first resistor. Thus, figure 2A shows all limitations of the claims except for a second half. However, Akita et al.'s figure 6 shows a circuit having plurality of half circuit connected in parallel for providing plurality of output signals. Therefore, it would have been obvious to one having ordinary skill in the art to add another Chau's figure 2A in parallel with it for the purpose of providing plurality of output signals.

Allowable Subject Matter

9. Claims 5, 20, 23, 26, 27, 30-32, 40, 48 and 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 37 and 38 are allowed.

Claims 5 and 20 would be allowable because the prior art fails to teach or suggest that the first and second impedances comprise resistors.

Claim 23 would be allowable because the prior art fails to teach first, second, and third bias current sources connected as claimed.

Claims 26 and 27 would be allowable because the prior art fails to teach or suggest the claimed detail and connection of the first and second current sources.

Claims 30-32 would be allowable because the prior art fails to teach the claimed detail of the transconductances.

Claim 40 would be allowable because the prior art fails to teach or suggest that one of the plurality of the switchable resistance stages is coupled between the first feedback loop and the second feedback loop when first, second, third and fourth switches are closed.

Claim 51 would be allowable because the prior art fails to teach or suggest the claimed detail of the switchable resistance stages.

Claims 37 and 38 are allowable because the prior art fails to teach or suggest that the feedback loop comprises amplifier coupled to the drain of the input transistor and to a floating voltage.

Conclusion

11 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

March 30, 2005